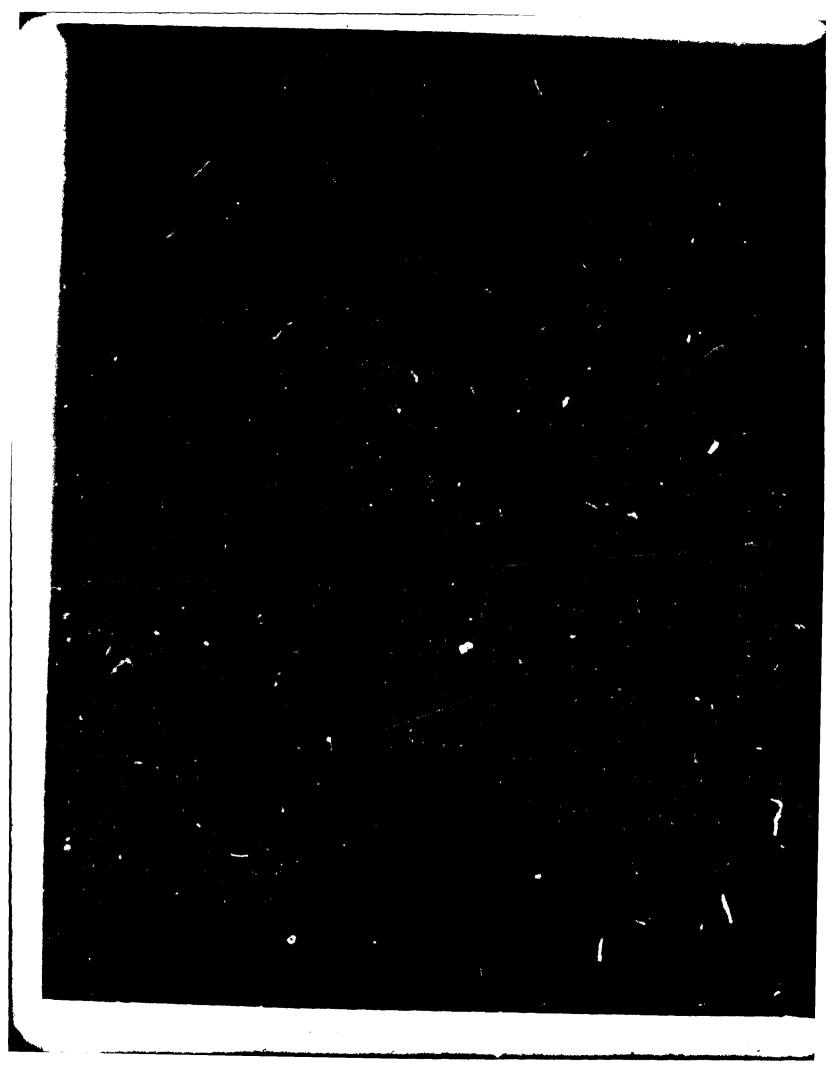


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MASSACHUSETTS INSTITUTE OF TECHNOLOGY LINCOLN LABORATORY

ADVANCED ELECTRONIC TECHNOLOGY

QUARTERLY TECHNICAL SUMMARY REPORT TO THE AIR FORCE SYSTEMS COMMAND

1 MAY - 31 JULY 1981

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LEXINGTON

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INTRODUCTION

This Quarterly Technical Summary covers the period 1 May through 31 July 1981. It consolidates the reports of Division 2 (Data Systems) and Division 8 (Solid State) on the Advanced Electronic Technology Program.

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DATA SYSTEMS DIVISION 2

INTRODUCTION

This section of the report reviews progress during the period 1 May through 31 July 1981 on Data Systems. Separate reports describing other work of Division 2 are issued for the following programs:

Seismic Discrimination	DARPA/NMRO
Distributed Sensor Networks	DARPA/IPTO
Network Speech Systems Technology	OSD-DCA
Digital Voice Processing	AF/ESD
Digital Voice Interoperability Program	AF/ESD
Packet Speech Systems Technology	DARPA/IPTO
Radar Signal Processing Technology	ARMY/BMDATC
Restructurable VLSI	DARPA/IPTO
Multi-Dimensional Signal Processing	AF/RADC

A.J. McLaughlin Head, Division 2 T. Bially

Associate Head

DIGITAL INTEGRATED CIRCUITS GROUP 23

1. INTRODUCTION

The first restructurable wafers, the phase 0 integrator, have been processed through first metal. We have now programmed and tested over 1000 amorphous Si-metal sandwich test structures without a failure. Unloaded nMOS ring oscillators with 10-nm nitrided oxide gates have operated with a 340-ps delay at 100 $\mu\mathrm{W}$ per stage. Experiments suggest that an electrochemical effect may be involved in MNOS fatigue.

II. ADVANCED CIRCUIT DESIGN AND SIMULATION

A. Phase 0 Integrator

The design of the phase 0 integrator, sometimes described as the RVLSI demonstration water has been finished, and reticles through first-level metal have been obtained. Processing of one run of waters has now reached first-level metal patterning. The remaining reticles will be available as needed for processing.

The reticles for first-level metal and above each consist of four patterns. These patterns are photocomposed onto the wafer using an aperture plate in the direct-step-on-wafer (DSW) machine to expose a different pattern on each of four passes over each wafer. Wiring and other features from one pattern merge with those in adjacent patterns to produce full-wafer photolithography. This has been tested and works well with 8-µm features, and should work with much smaller features.

B. RVLSI Spread-Spectrum Integrator

The first version of the integrator cell has been designed. The cell contains four 10-bit counters, two shift registers, and their associated pads and buffers. This version of the cell is complete with 1/O circuits which will make it possible to package cells for functional and performance testing. The cell contains approximately 2200 transistors and has an active area of 2.85% $1.58 \, \mathrm{mm}^2$.

In the complete, whole-water integrator the clock signals will be distributed to all 64 utilized cells. The associated interconnect capacitance is large and requires a very-wide CMOS driver. Such a clock driver has been designed with an effective output gate width of 3 mm for n-channel and 9 mm for p-channel.

The initial test wafer will contain integrator cells, driver cells, and standard test devices. The yield data for the clock driver will determine whether this approach is viable, or whether a distributed clock driver with a smaller amplifier in each integrator cell would be preferable.

C. FFT for Radar Applications

Mask design of the restructurable wafer-scale system for performing 16-point FFTs at a 16-MHz data rate is approaching completion. The basic cell is the multiplier-accumulator, of which four are required to make a single radix-two butterfly. A second cell type has been designed to perform a parallel-to-serial conversion of the data at the FFT input, and serial-to-parallel at the output. Recently, a significant effort has been to design a system of wafer interconnect that is suitable for the computational structure of the FFT.

The reticle to be used in wafer fabrication combines an array of four multiplieraccumulators, two versions of the data format converter cell (one with bonding pads and interconnect for wafer input, and the other for wafer output), and a final cell which contains process test devices. When the wafer is fabricated, the reticle will be shuttered such that only one of the above cells is exposed at a time. In this manner, the full set of different cell types for each lithographic level can be printed onto the wafer without changing the reticle.

HI. RESTRUCTURABLE VLSI (RVLSI) TECHNOLOGY

A. Laser-Formed Vias

Good yield statistics have been obtained on the regular a-Si insulated links (large area, no barrier layer). Over 4000 links have been formed with a 100-percent success rate at various power levels (above the threshold power) and a-Si thicknesses. Most connection resistances are <0.1 ohm (though some rise to 0.2 ohm). These test links carry 0.5 A before burning out.

The aim of the barrier-protected a-Si links (see previous Quarterly Technical Summary) is to retain the yield of the programmed a-Si links, while eliminating the failures due to Al-Si mixing during sinter. Link insulators of thin, 100-Å, oxide barriers sandwiching the a-Si-generated 0.1-ohm connections with a 20-percent threshold power increase over that of straight a-Si links. Increasing the oxide thickness generated a narrower useful power range, until at 500 Å no links <100-ohms were obtained. The oxide barrier structures have shown good resistance to both sinter and electrical breakdowns. Thin nitride or polyimide barriers were less successful.

Over 900 of the 20 × 20 µm² RVLSI laser links (see Ref. 1) have been tested and worked at laser power from 1.1 to 2.0 W. The single failure found was due to poor positioning. These connections carried up to 0.25 Å, with burnouts occurring in the 10-µm aluminum lines connecting the links, rather than in the via itself. In one demonstration, an already fabricated CMOS wafer had RVLSI links added to it. Then, laser connections were used to link in the power, signal in and signal out lines, and several ring oscillators were operated.

B. Via Reliability

Unprogrammed a-Si links have been subjected to 1400 h of electrical stress at 12 VDC and room temperature without degradation. Long-term thermal-stress tests of unprogrammed links

at 200° to 300°C and no voltage are about to begin.

C. Laser X-Y Table

A new pair of 2-in, travel tables is being fitted to the laser system. These tables will provide approximately four times the positional resolution of the present tables, with improved positional accuracy. Also, the planarity of the X-Y motion is to be improved to permit considerably greater focus accuracy.

D. Testing

Both a single mechanical probe for accessing cell pads and an optical probe for measuring the state of any CMOS pair are being designed to aid in the testing-restructuring process while the wafer is in place on the laser table.

IV. SEMICONDUCTOR PROCESSING

A. Lithography

A semiautomatic reticle aperture system discussed in Ref. 1 is nearly complete and will soon be tested. Until it is operational, we will use a manual version for some levels of the phase 0 integrator.

B. Reactive Ion Etching (RIE)

Experiments with a modified parallel-plate reactor for etching aluminum with BCL3 have successfully demonstrated the potential for achieving excellent anisotropy in the RIE system which should be relatively inexpensive, easily maintained, and provide fast turnaround time. This RIE system is currently being constructed, and is scheduled to undergo tests in the near future.

C. Polyimide

A study has been performed of first- to second-level metal via resistance with plasmaetched polyimide between-metal insulation. Vias are etched in O₂ plasma at 200-mTorr pressure. We found that this results in a very thin, insulating carbonaceous layer on the first metal. The use of $\rm O_2$ plasma at 50 mTorr to etch at least the final 20 percent of the polyimide in the vias eliminates this layer. This, followed by a dip in buffered HF to thin the oxide on the first-level aluminum, plus normal 425°C sinter, achieves a uniformly low-contact resistance of 0.2 to 0.3 ohm/via for 4- μ m² vias.

D. CMOS Test Chip

The 5- μ m CMOS process is being run repeatedly to gather data on yield and run-to-run variations in device parameters. At present, the variation in threshold voltage for a given run is ± 0.05 V, the nominal values for threshold voltage being ± 1 V. The present yield for gate arrays metallized as 4-bit counters is 50 percent. Experiments with reflowed phosphosilicate glass promise to improve yield in future runs.

A 4-bit serial-in, parallel-out CMOS dynamic shift register operated at clock frequencies as low as 16 Hz, implying storage times on the order of 0.25 s and storage-node leakage on the order of 0.5 pA at room temperature.

E. Nitrided Oxide Devices

The first depletion-load nMOS run using 10-nm nitrided oxide for the gate dielectric has been successfully completed. Not enough circuits have been tested to report yield statistics, but a check of several ring oscillators indicated few failures. The fastest ring oscillators (unloaded) have a 340-ps delay and a 0.4-mW power per stage, for a 140-fJ product, at 1.0-V power supply. The channel lengths of the enhancement and depletion devices were about 1 and 2 µm, respectively.

Evidence is accumulating that the relatively high fixed charge in nitrided oxides, about 5×10^{11} to 1×10^{12} cm⁻², is responsible for the low mobility in IGFETS using nitrided oxides. An empirical formula of Sun and Plummer² for

mobility vs fixed charge seems to fit our data very well. A series of annealing experiments is under way to attempt to correct this problem.

V. DEVICE THEORY

A. Fatigue-Induced Defects in MNOS and MOS Devices

Two types of defects which are related to MNOS fatigue have been found by etching fatigued devices in a 6-1-1 etch (nitric, hydrofluoric, and acetic acid) after removal of the aluminum electrodes. Since the etch attacks silicon and silicon dioxide at a rate greater than silicon nitride, defective regions in the nitride result in silicon etch pits. Nitride pinholes originally present in the film produce large etch pits and are believed to be related to early device failure. since such pits were found only in those devices which failed to survive 10⁶ write-erase cycles. The second type of defect was found within 7 nm of the silicon-dielectric interface and appeared as a general disintegration of the nitride where the extent of the disintegration correlated with the number of fatigue cycles. In addition, constant current stresses (total charge of 0.1 C/cm²) produced similar results, with an important exception. The etch resistance of the nitride was enhanced with positive bias and reduced with negative bias stresses. We suspect that this type of fatigue defect is electrochemical in origin. A similar result was seen using a MOS structure; in this case, a negative bias enhanced the etch resistance of the oxide.

In addition to fatigue studies, this etching procedure can be used as a process control technique for both nitride deposition and thermal oxidation.

B. The Electronic Structure of the N₄ Defect in Silicon Nitride

The N⁺₁ defect in silicon nitride is a singly charged nitrogen atom bonded to four nearestneighbor silicon atoms in a tetrahedral arrangement. The four electrons of the N_1^+ defect together with an electron from each of the four silicon atoms completely fill the bonding (valence) levels associated with the N_1^+ defect. An electron trapped on the N_1^+ defect ($N_1^+ + e + N_1^\circ$) must therefore occupy the lowest antibonding energy level of the unrelaxed N_1^+ defect. The electronic structure of this lowest antibonding level is described here.

The superbond-orbital method of Pantelides and Harrison³ and of Sokel⁴ was used to study a 17-atom cluster consisting of the N₄⁺ defect nitrogen atom, four nearest-neighbor silicon atoms, and twelve next-nearest-neighbor nitrogen atoms. Essentially, it was found that the trapped electron was not closely bound to the N₁⁺ nitrogen atom but distributed over the 17-atom cluster. Only 11.8 percent of the electron could be found on the unrelaxed N₁⁺ defect nitrogen atom. Most of the trapped electron (70 percent) was found on the four nearest-neighbor silicon atoms. The remaining 18.2 percent was found distributed evenly over the twelve next-nearest-neighbor nitrogen atoms. Of the 70 percent of the trapped electron found on the silicon atoms, most of that (97.6 percent) was found in Si(3s) atomic orbitals. The remainder of the 70 percent (2.4 percent) was found in Si(3p) atomic orbitals oriented in the direction of the N₁⁺ defect nitrogen. The picture of this trapped electron on the unrelaxed defect that emerges from the study, then, is not of a completely neutralized N₁⁺ defect nitrogen atom (N_1) , but of a partially neutralized one $(N_4^{+\,0.88})$, with most of the remaining electronic charge (-0.88e) distributed tetrahedrally ($T_{\rm d}$ symmetry) about the defect nitrogen on the nearest-neighbor silicon atoms.

How the N₁⁺ defect containing a trapped electron relaxes depends on whether or not the antibonding level of the trapped electron is degenerate. It can be shown by the superbondorbital method that the degeneracy of the trapped electron antibonding level depends on the interaction between the Si(3s) atomic orbitals and the three N(sp³) hybrid orbitals of the defect nitrogen that point away from any particular silicon atom. Unfortunately, the superbond-orbital method does not yield an accurate value for this interaction energy. However, it can be shown that if this interaction energy is in excess of 0.37 eV, the trapped electron antibonding level will be degenerate and relaxation will take place via the Jahn-Teller effect. If it is otherwise, the trapped electron level will be nondegenerate and relaxation will take place via a symmetric "breathing" mode.

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- R.J. Sokel, J. Phys. Chem. Solids <u>11</u>, 895 (1980).

COMPUTER SYSTEMS GROUP 28

A decision has been made to place control of the developing Lincoln Internal Data Link (LIDL) and implementation of the new ARPANET protocol in a single small machine to be connected to the central computer system. A DEC PDP-11/44 is being acquired and will be programmed to function as a gateway between the central computer, LIDL, and the ARPANET.

As previously reported, LIDL was originally conceived as a geographical extension of an Amdahl data channel. An AUSCOM interface unit, based on a DEC LSI/11, connects directly to the V/8 and responds to all input/output commands as though it were a standard control unit. On the outboard side, its Q-Bus sends and receives data via a Computrol modem and coaxial cable at speeds of up to 1 Mbps. A few Q-Bus computers, remotely located around the Laboratory, have been connected to the cable to test out the low-level transport software which has been developed for the AUSCOM.

As more devices are added to the system, it will be necessary to provide mechanisms for handling more complex communications functions such as addressing and message handling. These tasks will be assigned to the PDP-11/44.

Lincoln's unique hardware and software interfaces to the ARPANET were originally developed more than ten years ago. The hardware, which connects the Interface Message Processor (IMP) and an Amdahl channel, although relatively trouble free, has no regular maintenance support. The software cannot simply be modified to handle the new protocol, but must be rewritten. By placing the ARPANET interface function in an attached PDP-11/44, the Laboratory will have a vend \(\tau\)-supported hardware interface and access to a large community of users of compatible software.

A measurement package from Bell Northern Research has been installed to monitor usage patterns on the Conversational Monitor System (CMS). Early statistics, which have been limited to no more than 25 percent of the users to minimize overhead on the system, show consistency with past measurements. One of the major objectives of this activity is to increase our understanding of the nature of the interactive load, in order to continue to provide a responsive system, while addressing the need for better service for a growing batch load.

The rapid turnaround provided by the new on-line Benson Printer Plotters has had the effect of markedly increasing the volume of plotted output. In the first two weeks of operation, the total load processed equaled a typical large month of output from the COMp80 CRT plotter system. The COMp80 continues to provide publicationsquality occuput and photographic film, including movies of some plotted sequences.

SOLID STATE DIVISION 8

INTRODUCTION

This section of the report summarizes progress during the period 1 May through 31 July 1981. The Solid State Research Report for the same period describes the work of Division 8 in more detail. Funding is primarily provided by the Air Force, with additional support provided by the Army, DARPA, Navy, NASA, and DOE.

A.L. McWhorter Head, Division 8 I. Melngailis Associate Head

DIVISION 8 REPORTS ON ADVANCED ELECTRONIC TECHNOLOGY

15 May through 15 August 1981

PUBLISHED REPORTS

Journal Articles

JA No.			
5111	Infrared Spectroscopy Using Tunable Lasers	H.R. Schlossberg* P.L. Kelley	Chapter 1 in Spectrometric Techniques, G.A. Vanasse, Ed. (Academic Press, New York, 1981), Vol. 2, pp. 161-238
5129	A Comparison of Flash-Lamp- Excited Nd, La _{1-x} P ₅ O ₁₁ ($x =$ 1.0, 0.75, 0.20) Lasers	S.R. Chinn W.K. Zwicker*	J. Appl. Phys. <u>52</u> , 66 (1981)
5131	LiNbO ₃ Surface-Acoustic-Wave Edge-Bonded Transducers on ST Quartz and <001> Cut GaAs	D.E. Oates R.A. Becker	Appl. Phys. Lett. <u>38</u> , 761 (1981)
5154	Optical Interferometric Measurement of the Thermal Expansion of NdP ₅ O ₁₄	W.E. Barch S.R. Chinn W.K. Zwicker*	J. Appl. Phys. <u>52</u> , 3388 (1981)
5165	UV Photolysis of van der Waals Molecular Films	D.J. Ehrlich R.M. Osgood, Jr.	Chem. Phys. Lett. <u>79</u> , 381 (1981)
5166	Detectors for the 1.1 to 1.6 μm Wavelength Region	C.E. Hurwitz	Opt. Eng. <u>20</u> , 658 (1981)
5168	Anodic Dissolution Technique for Preparing Large Area GaAs Samples for Transmission Elec- tron Microscopy	J.P. Salerno J.C.C. Fan R.P. Gale	J. Electrochem. Soc. <u>128</u> , 1162 (1981)
5174	Liquid-Phase Epitaxial Growth of InP and InGaAsP Alloys	S.H. Groves M.C. Plonko	J. Cryst. Growth <u>51</u> , 81 (1981)
5175	Liquid-Encapsulated Czochralski Growth of InP Crystals	G.W. Iseler	J. Cryst. Growth <u>51</u> , 16 (1981)
5176	Vapor-Phase Epitaxy of GaInAsP and InP	P. Vohl	J. Cryst. Growth <u>54</u> , 101 (1981)

^{*} Author not at Lincoln Laboratory.

JA No.			
5185	Heteroepitaxy of Vacuum- Evaporated Ge Films on Single-Crystal Si	B-Y. Tsaur M.W. Geis J.C.C. Fan R.P. Gale	Appl. Phys. Lett. <u>38</u> , 779 (1981)
5189	The Electro-Optic Applications of InP	A.G. Foyt	J. Cryst. Growth <u>54</u> , 1 (1981)
5195	n ⁺ -InP Growth on InGaAs by Liquid Phase Epitaxy	S.H. Groves M.C. Plonko	Appl. Phys. Lett. <u>38</u> , 1003 (1981)
5215	Optical Properties of Proton Bombarded InP and GaInAsP	F.J. Leonberger J.N. Walpole J.P. Donnelly	IEEE J. Quantum Electron. QE-17, 830 (1981)
5219	GaAs Shallow-Homojunction Solar Cells on Ge-Coated Si Substrates	R.P. Gale J.C.C. Fan B-Y. Tsaur G.W. Turner F.M. Davis	IEEE Electron Device Lett. EDL-2, 169 (1981)
5220	Spatially Delineated Growth of Metal Films via Photochemical Prenucleation	D.J. Ehrlich R.M. Osgood, Jr. T.F. Deutsch	Appl. Phys. Lett. <u>38</u> , 946 (1981)
5225	Laser Chemical Technique for Rapid Direct Writing of Sur- face Relief in Silicon	D.J. Ehrlich R.M. Osgood, Jr. T.F. Deutsch	Appl. Phys. Lett. <u>38</u> , 1018 (1981)
5227	Transient Annealing of Arsenic- Implanted Silicon Using a Graphite Strip Heater	BY. Tsaur J.P. Donnelly J.C.C. Fan M.W. Geis	Appl. Phys. Lett. <u>39</u> , 93 (1981)
5229	Effect of Turbulence-Induced Correlation on Laser Remote Sensing Errors	D.K. Killinger N. Menyuk	Appl. Phys. Lett. <u>38</u> , 968 (1981)
5230	Temporal Correlation Measure- ments of Pulsed Dual CO ₂ Lidar Returns	N. Menyuk D.K. Killinger	Opt. Lett. <u>6</u> , 301 (1981)
5231	A Surface-Acoustic Wave/Metal- Oxide-Silicon Field-Effect Transistor Memory Correlator	D.L. Smythe R.W. Ralston	Appl. Phys. Lett. <u>38</u> , 886 (1981)
5242	MNOS/CCD Nonvolatile Analog Memory	R.S. Withers D.J. Silversmith R.W. Mountain	IEEE Electron Device Lett. EDL-2, 165 (1981)
5251	Sputtered Films for Wavelength- Selective Applications	J.C.C. Fan	Thin Solid Films <u>80</u> , 125 (1981)

Meeting Speeches

MS No.			
5321	Phase Diagram for LPE Growth of GalnAsP Layers Lattice Matched to InP Substrates	J.J. Hsieh	IEEE J. Quantum Electron. QE-17, 118 (1981)
5428	TEM Investigation of the Micro- structure in Laser-Crystallized Ge Films	R.P. Gale J.C.C. Fan R.L. Chapman H.J. Zeiger	Proc. MRS Mtg. 1980: Defects in Semiconductors (North-Holland, New York, 1981), pp. 439-411
5129	Scanning Cathodoluminescence Microscopy of Polycrystalline GaAs	J.P. Salerno R.P. Gale J.C.C. Fan J. Vaughan*	Proc. MRS Mtg. 1980: Defects in Semiconductors (North-Holland, New York, 1981), pp. 509-511
5678	Liquid Phase Epitaxial Growth of Hg _{1-x} Cd _x Te from Te-Rich Solutions	T.C. Harman	Proc. SPIE Vol. 285: Infrared Detector Materials (Society of Photo-Optical Instrumentation Engineers, Bellingham, Washington, 1981), pp. 84-91

UNPUBLISHED REPORTS

Journal Articles

JA No.			
5186	Solid-Phase Epitaxial Crystallization of Amorphous Ge on <100>Si	B-Y. Tsaur J.C.C. Fan J.P. Salerno C.H. Anderson R.P. Gale F.M. Davis E.F. Kennedy* T.T. Sheng*	Accepted by J. Electrochem. Soc.
5218	Efficient Si Solar Cells by Low-Temperature Solid-Phase Epitaxy	B-Y. Tsaur G.W. Turner J.C.C. Fan	Accepted by Appl. Phys. Lett.
5240	Improved Techniques for Growth of Large-Area Single-Crystal Si Sheets over SiO ₂ Using Lat- eral Epitaxy by Seeded Solidification	B-Y. Tsaur J.C.C. Fan M.W. Geis D.J. Silversmith R.W. Mountain	Accepted by Appl. Phys. Lett.

^{*} Author not at Lincoln Laboratory.

JA No.			
5243	Ultrathin, High-Efficiency Solar Cells Made from GaAs Films Prepared by the CLEFT Process	C.O. Bozler R.W. McClelland J.C.C. Fan	Accepted by IEEE Electron Device Lett.
5245	Mixing of 10 μm Radiation in Room Temperature Schottky Diodes	P.E. Tannenwald H.R. Fetterman C. Freed C.P. Parker B.J. Clifton R.G. O'Donnell	Accepted by Opt. Lett.
5217	Remote Probing of the Atmosphere Using a CO ₂ DIAL System	D.K. Killinger N. Menyuk	Accepted by IEEE J. Quantum Electron.
5253	Direct Writing of Refractory Metal Thin Film Structures by Laser Photodeposition	D.J. Ehrlich R.M. Osgood, Jr. T.F. Deutsch	Accepted by J. Electrochem. Soc.
	Meel	ting Speeches*	
MS No.			
5084A	Surface-Acoustic-Wave Devices for Analog Signal Processing	S.A. Reible	Seminar, Dept. of Elec- trical and Computer En- gineering, University of Massachusetts, Amberst, 6 May 1981
5145B	Recent Experimental Results on Permeable Base Transistors	C.O. Bozler	
5498D	On the Use of AsH ₃ in the MBE Growth of GaAs	A.R. Calawa	Workshop on GaAs Microstructures and High Performance Devices, Boston,
5718	High-Speed InP Optoelectronic Switches for Signal Processing Applications	F.J. Leonberger A.G. Foyt R.C. Williamson	8-10 June 1981
5525	A New Technique for Preparing p-n Junctions for Si Photo- voltaic Cells	J.C.C. Fan T.F. Deutsch G.W. Turner D.J. Ehrlich R.L. Chapman R.M. Osgood, Jr.	15th IEEE Photovoltaic Specialists Conf., Orlando, Florida, 11-15 May 1981

^{*} Titles of Meeting Speeches are listed for information only. No copies are available for distribution.

MS	No.

313 140,		
5526	Preparation of Heteroepitaxial Ge Films on Single-Crystal Si as Low-Cost Substrates for Ef- ficient GaAs Solar Cells	B-Y. Tsaur J.C.C. Fan R.P. Gale
5531	GaAs Shallow-Homojunction Solar Cells on Epitaxial Ge Grown on Si Substrates	R.P. Gale B-Y. Tsaur J.C.C. Fan F.M. Davis G.W. Turner
5533	GaAs Shallow-Homojunction Con- centrator Solar Cells	G.W. Turner J.C.C. Fan R.L. Chapman R.P. Gale
5672	Junction Formation by Solid- Phase Epitaxy: A Novel Low- Temperature Technique for Efficient Si Solar Cells	B-Y. Tsaur G.W. Turner J.C.C. Fan
5726	Thin-Film GaAs Solar Cells	J.C.C. Fan C.O. Bozler R.W. McClelland
5558A	Techniques for Electron Beam Testing and Restructuring Integrated Circuits	D.C. Shaver
5634A	A Novel Anisotropic Dry Etching Technique	M.W. Geis G.A. Lincoln N.N. Efremow
5656	Application of ≈ 100Å Linewidth Structures Fabricated by Shad- owing Techniques	D.C. Flanders A.E.White
5657	A Simple Technique for Modify- ing the Profile of Resist Exposed by Holographic Lithography	N.N. Efremow N.P. Economou K. Bezjian* S. Dana* H.I. Smith*
5658	Experimental Evaluation of Interferometric Alignment Techniques for Multiple Mask Registration	T.M. Lyszczarz D.G. Flanders N.P. Economou P.D. DeGraff
5661	High Resolution Ion Beam Lithography	N.P. Economou D.C. Flanders J.P. Donnelly

15th IEEE Photovoltaic Specialists Conf., Orlando, Florida, 11-15 May 1981

16th Symposium on Electron, Ion and Photon Beam Technology, Dallas, Texas, 26-29 May 1981

^{*} Author not at Lincoln Laboratory.

MS No.			
5723	Prospects for High-Brightness X-Ray Sources for Lithography	N.P. Economou D.C. Flanders	16th Symposium on Electron, Ion and Photon Beam Tech- nology, Dallas, Texas, 26-29 May 1981
5563	Sputtered Films for Wavelength- Selective Applications	J.C.C. Fan	Intl. Conf. on Ion and Plasma Assisted Techniques, Amsterdam, The Netherlands, 30 June – 2 July 1981
5571A	MNOS/CCD Nonvolatile Analog Memory	R.W. Withers D.J. Silversmith R.W. Mountain	
5632B	InP Optoelectronic Mixers	A.G. Foyt F.J. Leonberger R.C. Williamson	38th Annual Device Research Conf., Santa
5717	High Quality MOSFETS on Silicon Films Prepared by Zone Melting Recrystallization of Encapsu- lated Polysilicon on SiO ₂	M.W. Geis B-Y. Tsaur J.C.C. Fan D.J. Silversmith R.W. Mountain J.P. Donnelly E.W. Maby* D.A. Antoniadis*	Barbara, California, 22-24 June 1981
5572	Fabrication of Multiple- Branching Single-Mode Wave- guide Circuits in LiNbO ₃	F.J. Leonberger L.M. Johnson*	31st Electronic Components Conf., Atlanta, Georgia, 11 May 1981
5572A	Applications of Integrated Optics	F.J. Leonberger	Integrated Optics Seminar, Abbott Labs., No. Chicago, Illinois, 29 May 1981
5574	Chemical Vapor Deposition of Epitaxial GaAs on Ge-Coated Si Substrates	R.P. Gale F.M. Davis B-Y. Tsaur J.P. Salerno G.W. Turner J.C.C. Fan	5th Intl. Conf. on Vapor Growth and Epitaxy. Coronado, California. 19-24 July 1981
5617	Graphoepitaxy of Vacuum- Evaporated Ge Films on Cr/Au-Coated Amorphous SiO ₂ Substrates	B-Y. Tsaur M.W. Geis	1 2 - 6 1 gary 1 201

^{*} Author not at Lincoln Laboratory.

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MS No.		
5618	Lateral Growth of Single- Crystal InP Over Dielectric Films by Orientation-Dependent VPE	P. Vohl C.O. Bozler R.W. McClelland A. Chu A.J. Strauss
5626	Growth of Laser-Quality MgF ₂ Crystals Doped with Ni. Co. or V	R.E. Fahey P.F. Moulton
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⁵th Intl. Conf. on Vapor Growth and Epitaxy. Coronado, California, 19-24 July 1981

Electronic Materials Conf., Santa Barbara, California, 24-26 June 1981

^{*} Author not at Lincoln Laboratory.

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5685	Rapid Direct Writing of Surface Relief Structures in Silicon Using Laser Photoetching	D.J. Ehrlich R.M. Osgood, Jr. T.F. Deutsch	Electronic Materials Conf., Santa Barbara, California, 24-26 June 1981
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5707. A	Laser Microchemistry for Electronics	D.J. Ehrlich R.M. Osgood, Jr. T.C. Deutsch	Laser Workshop, M.I.T., 1-5 May 1981: Naval Re- search Laboratory, Washington, DC, 11 May 1981
5732	GaInAsP Laser Program at Lincol (Laboratory	* V. Walpole	Fiber Optics Sensor System (FOSS) Workshop, Fort Eustis, Virginia, 28 May 1981

SOLID STATE DIVISION 8

I. SOLID STATE DEVICE RESEARCH

Phase diagram analyses of the liquid-phase epitaxial (LPE) growth of Hg_{1-x}Cd_xTe have been carried out to determine the interrelationships between growth solution composition, mercury vapor pressure, and growth temperature for various operational steps during the LPE growth cycle. The results indicate that it should be possible to grow good-quality epilayers of this material.

Carrier concentrations in the low 10¹⁶ cm²³ range and electron Hall mobilities over 10⁵ cm²/V-s at 77 K have been achieved in annealed LPE-grown Hg_{1-x}Cd_xTe layers, with x in the 0.1 to 0.2 range. In the same range of x, the material constant that links layer thickness to growth time, number of degrees supercooling, and ramp rate has been determined to be approximately 0.75 μm/°C-min. ¹⁻².

A technique has been developed to monolithically integrate a passive waveguide with a GalnAsP/InP double-heterostructure laser for potential use in fabricating modulators and integrated external cavities. Initial tests of broad-area lasers with 100-μm passive waveguide sections showed threshold current densities of 2.4 to 3.1 kA/cm².

The feasibility of fabricating permeable-base transistors by molecular-beam epitaxial (MBE) growth of GaAs over tungsten gratings is being explored. By using a substrate temperature of 680°C and an As₂/Ga ratio of 10, sufficient surface migration of the GaAs was achieved to permit the first single-crystal MBE growth of GaAs over amorphous tungsten gratings.

II. QUANTUM ELECTRONICS

A differential-absorption LIDAR (DIAL) system has been utilized to detect the exhaust pollutants (CO and C_2H_1) emitted by an A-10 jet

aircraft at a range of 2.7 km. Concentrations of $\rm C_2H_4$ were measured as the aircraft engines were started, run at fast idle, and shut down, with the greatest concentrations observed at shutdown. An increase in the concentration of CO was observed during engine startup and idle.

A pulse-pumped Co:MgF $_2$ laser, cooled to 77 K, has generated up to 150 mJ of output energy per pulse and has been tuned between 1.596 and 2.288 μm_s a 2000-cm $^{-1}$ range. Room-temperature pulsed operation of a Ni:MgO laser, the first Ni:CAMGAR (CaY $_2$ Mg $_2$ Ge $_3$ O $_{12}$) laser, and CW tunable laser action from V:MgF $_2$ have also been demonstrated. (See also Sec. III.)

The spectral width of CW, single-frequency GaAlAs diode lasers has been observed to saturate at high power levels due to refractive index fluctuations. These index fluctuations are thought to arise from electron number fluctuations in the small laser gain volume.

The electrical properties of single-crystal and amorphous Si, doped using a pulsed UV laser, have been studied as a function of laser wavelength and fluence, and of UV dose. Dissociation of molecules adsorbed on the Si surface can supplement photolysis of gas-phase molecules as a source of doping atoms.

An investigation of the properties of superconducting-insulator-superconducting (SIS) diodes in the submillimeter has been initiated using Nb-Nb₂O₅-Pb devices fabricated on quartz. Mixing between the fifth harmonic of a 69-GHz klystron and a 345-GHz carcinotron yielded an IF with a 30-dB signal-to-noise ratio.

III. MATERIALS RESEARCH

Continuous single-crystal Si sheets over SiO_2 with areas of several square centimeters have been produced from polycrystalline Si films by two improved versions of the LESS technique (lateral epitaxy by seeded solidification) that use a composite $\mathrm{Si}_3\mathrm{N}_4/\mathrm{SiO}_2$ encapsulating layer.

N-channel MOSFETs fabricated in these films exhibit electron surface mobilities in the range of 600 to 700 cm²A·s., comparable to the values for devices fabricated in bulk Si.

Solid-phase epitaxial Si layers that are strongly p-type have been grown at 400° to 500°C by transport of Si atoms from an amorphous Si film through an Al film deposited on n-type Si substrates. This low-temperature process, which produces good rectifying junctions between the epitaxial layers and their substrates, has been used in the fabrication of solar cells with conversion efficiencies at AVII of 10.4 and 8.5 percent on <100>Si and polycrystalline Si substrates, respectively, without an antireflection coating or back-surface field structure.

As part of a study of the lateral growth of InP layers over dielectric films by vapor-phase epitaxy, the rates of vertical growth by the PCl₃-InP-H₂ method on the four principal low-index planes have been determined as a function of substrate temperature for a source temperature of 700°C. For each substrate orientation, the growth rate exhibits a maximum between 620° and 660°C; up to 670°C, the rate increases in the order [111]B, [100], [111]A, [110].

A theoretical model has been developed to describe the crystallization of a thin amorphous semiconductor film, supported on a thick substrate, that is irradiated by a heat pulse from a cylindrically symmetric energy beam. Solution of the integral equation for the dynamics of the amorphous-crystalline boundary radius yields three alternative types of motion – a series of jumps, a single longer jump, or indefinite runaway – that account for structural features observed in pulsed laser and electron-beam crystallization.

A gradient-freeze technique employing self-sealing graphite crucibles has been used to grow single crystals of MgF₂, doped with Ni. Co. or V. up to 3.7 cm in diameter and 10 cm long. High-quality laser rods up to 5 cm long have been fabricated from these crystals.

IV. MICROELECTRONICS

A charge-coupled device (C.O) implementation of a time-integrating correlator has been designed for use with the GPS (Global Positioning System) P-code which will require that the CCD be clocked at 20.46 MHz, or twice the P-code bit rate. The device uses a pipe-organ structure to achieve high-speed operation, and a complementary input structure to avoid signal- and code-dependent offsets.

A new CCD parallel-processing architecture has been developed which can perform many high-level mathematical functions such as vector-matrix, matrix-matrix, and triple-matrix products. The basic device consists of a floating-gate CCD tapped delay line and parallel arrays of CCD signal processors. All computations are performed in the charge domain, and each is the multiplication of a sampled analog data point with a digital word.

An optimized process for the high-resolution etching of aluminum on oxidized silicon waters using a BCl₃ plasma has been developed. Constant plate-to-plate voltage and nonstandard system geometries have been used to achieve unform etching with clean, vertical walls and no residues.

3200-A-period gratings, several-thousandangstroms deep, have been etched in siliconusing reactive ion etching with an ArSiCl₁O₂ gas mixture and abuninum or nickel as the etchmask material. Redeposition of SiO₂ during etching creates a keyhole cross section in the etched grooves when using an aluminum mask, and this phenomenon becomes more pronounced as the aluminum mask is made thicker.

Electron-beam techniques have been developed for defect location and adaptive interconnection on wafer-scale integrated systems. These techniques are compatible with a commercially available electron-beam lithography system and standard nMOS wafer processing. Test structures

including an electron-beam multiplexer, floatinggate transistors, and simple FETs were designed, fabricated, and tested.

The feasibility of using integral microstrip transmission lines for interconnecting GaAs microwave devices has been demonstrated using a simulated mixer application. This fabrication technique, which employs a polyimide dielectric layer, permits direct electrical contact to the devices, and should substantially reduce the complex assembly procedures currently required by such devices.

V. ANALOG DEVICE TECHNOLOGY

A SAW delay line has been developed with very high (>100 dB) isolation between the short

(10-ns) pedestal-of-delay acoustic signal and the direct electrical feedthrough signal by using edge-bonded transducers in a dual-track geometry. The high feedthrough isolation design provides the first practical means of providing high-performance SAW transversal filters with very short-delay pedestal.

A comprehensive analysis has been made of the performance limits of integrated optical spectrum analyzers. Resolution is found to be limited to around 2.7 MHz, and the time-bandwidth product to approximately 1000 with existing detector arrays. The aperture and weighting for the input lens are shown to be important with regard to resolution, crosstalk, and scalloping loss.

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